PARTIAL ARRAY SELF-REFRESH

This application is a Continuation of U.S. Application No. 09/988,988, filed November 19, 2001, now US Patent No. 6,650,587 which is incorporated herein by reference.

Technical Field of the Invention

The present invention relates to integrated circuits and in particular to a refresh operation in a memory device.

Background of the Invention

Memory devices such as dynamic random access memory (DRAM) devices are widely used to store data in computers and electronic products.

A typical DRAM device has many memory cells. Each memory cell is capable of storing a bit of data. The value of the data in each memory cell is determined by the value of a charge held by the memory cell. As a known electrical property, charge loses its value over time due to leakage and other factors, causing data to become invalid. Therefore, to retain the validity of the data, the memory cells are periodically refreshed to keep the charges at their original values.

In a typical DRAM device, the memory cells are refreshed during a refresh mode, in which all memory cells are refreshed regardless of whether all or only a portion of the memory cells contain useful data. Therefore, refreshing all memory cells during the refresh mode is not efficient.

For these and other reasons stated below, and which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need for an efficient method to refresh memory cells in a memory device.